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S11	10	703/20.ccls. and @PD>"20080701"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2008/11/04 13:23
S12	236	soc and verif\$7 and ((test adj bench) or testbench)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2008/11/04 13:26



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K Albin, M Inc, TX Austin - Design Automation Conference, 2001. Proceedings, 2001 - [ieeexplore.ieee.org](#)  
... 3.1.3 **SoC** designs are large and complex, and so is the ... 3.2 Interface Monitors Figure 1 shows the basic components of a unit-level **verification testbench**. ...

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P Rashinkar, P Paterson, L Singh - 2001 - [books.google.com](#)

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G Mosensson - Proceedings of DATE User Forum, 2000 - [cecs.uci.edu](#)

... effect they have on the design of the **testbench**. The rest of this paper focuses on showing practical and novel approaches to the **verification** of **SOC** designs. ...

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... **TESTBENCH** Emulated System Monitors ... the processor RTL, the **verification** suite, and the system **test-bench**. ... be easily merged into an **SOC verification** environment. ...

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 ... done: the state space is way too large to exhaustively **test** it, and ... 5. CONCLUSIONS

 The fundamental problem that **SoC** and **Core verification** efforts deal with ...

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